The specification has been amended to make editorial changes including adding a new title to place the application in condition for allowance at the time of the next Official Action.

Claims 1-12 were previously pending in the application. New claims 13 and 14 are added. Therefore, claims 1-14 are presented for consideration. Claims 1, 8 and 9 are amended to address the claim objections noted in the Official Action.

Claims 1-3, 7 and 8 are rejected as anticipated by POCHOLLE et al. 4,917,450. This rejection is respectfully traversed.

Claim 1 of the present application recites a plurality of processing elements and a switcher that connects each of the plural processing elements to each other.

As shown in Figure 3 and as disclosed on page 9, lines 21-25 of the present application, a switcher 110 is directly connected to the network interfaces 111, 111, 113 and 114 of the processors 101, 102, 103 and 104 to provide a communication function between the processors. Accordingly, the switcher 110 provides communication between each of the processors 101, 102, 103 and 104.

In contrast, column 3, lines 3-11 of POCHOLLE et al. disclose that central processing unit 1 of processing units 1-8 may communicate with the memory RAM by means of a data emitter/receiver 21 with a data emitter/receiver 22 located in the RAM. Column 1, lines 32-40 of POCHOLLE et al. disclose that

selected ones of several circuits connect to other selected circuits by means of a light beam diffracted in a direction chosen from one of several pre-defined directions. There is no teaching or suggestion that each of CPU1-8 communicates with each other. Accordingly, POCHOLLE et al. do not disclose or suggest that a switcher connects each of the plural processing elements to each other as recited in claim 1 of the present application.

Claims 2, 3, 7 and 8 depend from claim 1 and further define the invention and are also believed patentable over POCHOLLE et al.

Claims 1-5 and 7 are rejected as anticipated by LEVI et al. 5,148,504. This rejection is respectfully traversed.

Claim 1 of the present application recites a single switcher that connects each of the plural processing elements to each other.

In contrast, as seen in Figure 10 of LEVI et al., for example, a plurality of switchers 108 connect a plurality of integrated circuits 102, 103 (processing elements). In addition, column 13, lines 24-29 of LEVI et al., for example, disclose that selective coupling of input signals into guides 106 of optical bus 107 is controlled by optical switch logic by means not shown at junctures 108. Accordingly, input signals are sent from optical switcher 108 to each of integrated circuits 102, 103. LEVI et al. do not disclose or suggest that the switcher 108 provides a communication function between the processors 102, 103

or that the single switcher connects each of the plural processing elements to each other as recited in claim 1 of the present application. As the reference does not disclose that which is recited, the anticipation rejection is not viable. Accordingly, reconsideration and allowance of claim 1 are respectfully requested.

Claims 2-5 and 7 depend from claim 1 and further define the invention and are also believed patentable over the cited prior art.

Claims 1 and 6 are rejected as anticipated by CARLSON et al. 5,506,961. This rejection is respectfully traversed.

Claim 1 of the present application recites a single switcher that connects each of the plural processing elements to each other.

By way of example, Figure 3 of the present application shows processing elements 101, 102, 103 and 104 connected through the switcher 110 to each other.

In contrast, Figure 1 of CARLSON et al. shows a central processing unit 105 (indicated in the Official Action as a switcher) and a plurality of input output processors 120. As disclosed on column 5, lines 1-6, the input/output processors 120 are connected to the central processing unit 105 by input/output bus 115. Accordingly, CARLSON et al. disclose what is shown in prior art Figure 1 of the present application, processing elements connected to a bus, not a single switcher that connects

each of the plural processing elements to each other as recited in claim 1 of the present application.

Claim 6 depends from claim 1 and further defines the invention and is also believed patentable over CARLSON et al. In addition, claim 1 recites a single switcher. The Official Action has indicated at least two switchers 105, 110 and also switcher 112 which is part of 110.

Claims 1 and 9-11 are rejected as anticipated by YOSHIMURA et al. 6,343,171. This rejection is respectfully traversed.

As noted above, claim 1 recites a single switcher. The Official Action has denoted two switchers 26a, 26b. The plural switchers 26a, 26b are not a single switcher that connects each of the plural processing elements to each other as recited in claim 1 of the present application. As the reference does not disclose that which is recited, the anticipation rejection is not viable. Reconsideration and allowance of claim 1 are respectfully requested.

Claims 9-11 depend from claim 1 and further define the invention and are also believed patentable over the cited prior art.

New claim 13 recites that each of the plural processing elements are only connected to the single switcher, through each respective network interface. New claim 14 recites a plurality of peripheral input/output processing elements, a core processor

and a single switcher that connects each of the plural peripheral processing elements and the core processor to each other. These features are not disclosed in the references.

Accordingly, it is believed that the new claims avoid the rejection under §102 and are allowable over the art of record.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

Attached hereto is a marked-up version showing the changes made to the title, specification and claims. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

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"VERSION WITH MARKINGS TO SHOW CHANGES MADE"

IN THE TITLE:

The title has been amended as follows:

--SEMICONDUCTOR DEVICE PACKAGE HAVING A SWITCHER CONNECTING PLURAL PROCESSING ELEMENTS--.

IN THE SPECIFICATION:

Page 3, the paragraph, beginning on line 24, has been amended as follows:

--According to a first aspect of the invention, there is provided a semiconductor device which comprises a plurality of processing elements; and a switcher which connects the elements to each other. Wherein, each of the processing elements includes a network interface and is connected to the switcher via the network interface.--.

Page 4, the paragraph, beginning on line 27, bridging pages 4 and 5, has been amended as follows:

--According to a sixth aspect of the invention, the semiconductor device further comprises a plurality of semiconductor chips each of which includes the plurality of processing elements and the switcher, and at least one inter-switcher which connects the semiconductor chips to each other. The configuration is desirable to constitute a plurality of packages by using many semiconductor chips.--.

Page 5, the paragraph, beginning on line 4, has been amended as follows:

--According to a seventh aspect of the invention, the plurality of semiconductor chips and the inter-switcher are implemented two-dimensionally. In addition, the inter-switcher is located in one of the plurality of semiconductor chips, and the semiconductor chips are implemented three-dimensionally. Also, each of the switcher and the inter-switcher may be a circuit switching.--.

Page 10, the paragraph, beginning on line 16, has been amended as follows:

--The package 301 and the plurality of the packages 201 and 202 are connected to each other via an extra communication port 320 which is located outside the package. This is the difference between the system LSI shown in Fig. 4 and the system LSI shown in Fig. 5. Also, the package 301 includes an intra-switcher 313 which internally connects a plurality of processing modules 311 and 312, and an inter-switcher 314 which connects the packages. The processing modules 311 and 312 include network interfaces 315 and 316, respectively.--.

Page 11, the paragraph, beginning on line 10, has been amended as follows:

--In Fig. 6, a system LSI is shown which is composed of a single chip module produced by forming a die 410 made from a silicon wafer 400 in a package 420. In the die 410, there are a switcher 412 located at the center of the die and a plurality of

processing modules 411 located around the switcher. The die can perform the same functions as the system LSI shown in Fig. 3.--;

the paragraph, beginning on line 26, bridging pages 11 and 12, has been amended as follows:

--The package 600 is based on a multi-chip module forming a plurality of semiconductor chips 610 on a surface of a package substrate 601. Around the multi-chip module, sealing is done by a sealing resin 602. Further, a sealing resin 603 is used to seal the substrate 601 and the sealing resin 602. As a result, a light signal 620 from a light emitting element 611 is confined inside the sealing resin 602.--.

IN THE CLAIMS:

Claim 1 has been amended as follows:

--1. (amended) A semiconductor device comprising:

a plurality of processing elements; and

a single switcher [which] that connects each of the plural processing elements to each other,

wherein each of the plural processing elements includes a network interface and is connected to the single switcher via the network interface.--

Claim 2 has been amended as follows:

--2. (amended) The semiconductor device of claim 1, wherein the plural processing elements are located around the single switcher.--

Claim 4 has been amended as follows:

--4. (amended) The semiconductor device of claim 1, wherein the plural processing elements and the single switcher are implemented in a single semiconductor chip.--

Claim 5 has been amended as follows:

--5. (amended) The semiconductor device of claim 1, wherein the plural processing elements and the single switcher are implemented in a single package.--

Claim 6 has been amended as follows:

--6. (amended) The semiconductor device of claim 1, wherein one of the plural processing elements and the single switcher are connected by peer-to-peer connection via at least one transmission line.--

Claim 7 has been amended as follows:

--7. (amended) The semiconductor device of claim 1, wherein each of the plural processing elements has a function of the same hierarchical level.--

Claim 8 has been amended as follows:

--8. (amended) The semiconductor device of claim 1, wherein at least one of the plural processing elements and the single switcher are located in a space where [the] light is confined, and each of the at least one of the plural processing [element] elements and the single switcher has a light emitting

element and a light receiving element, [thereby] wherein an optical communication is performed between the at least one of the plural processing [element] elements and the single switcher.--

Claim 9 has been amended as follows:

--9. (amended) The semiconductor device of claim 1 further comprising:

a plurality of semiconductor chips each of which includes [the plurality of] plural processing elements and [the] a single switcher; and

at least one inter-switcher which connects the semiconductor chips to each other.--

Claim 10 has been amended as follows:

--10. (amended) The semiconductor device of claim 9, wherein the [plurality of] plural semiconductor chips and the inter-switcher are implemented [two-dimensionally] on a single package.--

Claim 11 has been amended as follows:

--11. (amended) The semiconductor device of claim 9, wherein the inter-switcher is located in one of the [plurality of] plural semiconductor chips, and the plural semiconductor chips are implemented [three-dimensionally] on a plurality of stacked packages.--